31.6 A 1GS/s 11b Time-Interleaved ADC in 0.13μm CMOS

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A time-interleaved ADC architecture that eliminates the need to correct timing offsets and is yet scalable to high sampling rates is presented. This 1GS/s 11b ADC has 55dB peak SNDR, consumes 250mW power, and occupies 3.5mm^2 area.

Time-interleaved ADCs suffer from gain mismatch, offset and timing mismatch errors between the individual sub-sampled ADCs (Sub-ADCs). Gain and offset errors can be corrected using traditional techniques [1, 2, 3]. In the architecture presented in [2], an input S/H at the highest sampling rate of the ADC, f_s, eliminates the need for timing error correction. However, this structure has at least two disadvantages. Firstly, it limits the bandwidth and linearity of the high-speed sampling in the S/H. This is because the sub-sampled sampling networks of typically N/2 Sub-ADCs (assuming there are N Sub-ADCs) load the high-speed sampler during its track period. Secondly, the Sub-ADCs input signal is held for a short time period T, equal to $1/f_s$, making the input stage design of the Sub-ADC difficult and the ADC less scalable at high speeds.

In another architecture, instead of having a S/H operating at f_s, N (N≥2) sub-sampled S/H (Sub-S/H) circuits may be used for N Sub-ADCs, reducing the highest sampling rate to f_s/N and making the architecture scalable to higher sampling rates. The disadvantage is that this requires timing error correction through complicated signal processing techniques which can have severe limitations for broadband input signals [1]. Furthermore, residual misalignment after calibration can still limit performance [3]. Finally, the loading of the Sub-S/Hs limits the achievable bandwidth and power of its pre-driver [3]. These two architectures are shown in Fig. 31.6.1.

In this paper, a time-interleaved ADC architecture is presented that achieves the better of the two above mentioned architectures. The block diagram of this architecture is shown in Fig. 31.6.2. The first sampling is done at f_s through a switch followed by an array of Sub-S/H circuits. A timing technique and a sampling network is devised such that it achieves the following three functions thereby mitigating the disadvantages of the prior two architectures and resulting in a low-power design [4].

Firstly, no more than one of the Sub-S/Hs loads the first sampling switch for any appreciable time, thereby its achievable bandwidth and linearity is not limited.

Secondly, to ensure that timing mismatch in Sub-S/Hs does not limit the SNR, the turn-off of the clock performing the sampling in the Sub-S/Hs is done during the off phase of the first sampling switch. Based on the above two functions, the on-period of the Sub-S/Hs sampling is kept lower than T.

Thirdly, double sampling is used to maximally utilize the power of amplifiers in the ADC in both of the phases of the sub-sampled clock. This architecture thus requires only N/2 Sub-S/Hs and Sub-ADCs having two sub-sampled clocks each, at a frequency of f_s/N, and results in reduced total power.

The time-interleaved ADC is shown in Fig. 31.6.3. To achieve high linearity, the first switch driven by f_s clock, is bootstrapped. The timing of the Sub-S/H clocks and f_s, to achieve all of the three functions described above, is shown in Fig. 31.6.4. Each of the N/2 circuits has two out-of-phase clock sets, p1x (p1e, p1_s, p1) and p2x (p2e, p2_s, p2) to achieve double sampling. The first sampling switch is driven by the f_s clock. The on-period of the first sampling in the jth Sub-S/H is defined by the simultaneous turn on of switches driven by both p1e<j> and p1_s<j> (or p2e<j> and p2_s<j>, conversely) and is thus less than T (see Fig. 31.6.4). The transfer of the sampled charge to the output of the Sub-S/H occurs during the turn on of both p2 <j> and p2_e<j> (or p1 <j> and p1_e<j> conversely).

In this design, N=8, and thus 4 Sub-S/H and Sub-ADC circuits are used. The Sub-ADC is implemented using 11b pipelined converters to keep the contribution of quantization noise negligible as compared to the device noise, for a SNR specification of ~58dB. The pipelined architecture is a three-stage design resolving 3.5 bits in the first two stages and 5 bits in the last stage. Multi-bit design improves the SFDR for a given total capacitor value in the MDAC [5]. Thus, the sampling capacitor value is limited by kT/C noise requirements, rather than matching. This lowers the area and power of the Sub-ADC. Resolving 3.5 bits in the first two stages reduces the error-correction range, but is possible to implement because the input signal to the MDAC is sample and held, which significantly relaxes the clock skew requirement between the flash converter and the sampling network in the MDAC. Careful optimization of amplifier architecture and design results in only 35mW power for each Sub-ADC.

For test purposes, the gain and offset error correction is done in software. The offsets of the Sub-ADC output codes are removed by subtracting the mean, and the gains of each Sub-ADC output are scaled with respect to the rms value of the codes, before combining the output codes. Figure 31.6.5 shows that for a 5MHz input at 1GHz sampling rate, the ADC has 54.9dB SNDR and 58.5dB SFDR. A two-tone test in Fig. 31.6.5 indicates inter-modulation distortion for dual-tone frequencies of 470 and 471MHz to be less than 53.1dB. The DNL and INL plot for this 1GS/s 11b ADC, designed for ~55dB SNDR performance, is also shown in Fig. 31.6.5. The timing architecture described herein results in spectral tones lower than -65dB without requiring any timing offset correction. Figure 31.6.6 shows that this ADC has a DR greater than 60dB and maintains high SNDR of 52 to 55dB for wideband input frequencies. Figure 31.6.7 shows the zoomed in micrograph of the ADC.

The ADC is implemented in a 0.13μm 1.2V/2.5V logic CMOS process. The peak SNR is 58.6dB and the peak SNDR is 55dB. The ADC has 52dB SNDR at 400MHz input frequency. The conversion efficiency, defined by power/(2^{ENOB}×2×ERBW) is better than 0.5pJ/conversion-step. This ADC has the highest SNDR, SNR and linearity for any reported ADC sampling >500MS/s, and the lowest reported power for any ADC comparable to its accuracy and speed.

References:

[1] S. Jamal et al., "A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter with Digital Background Calibration," *IEEE J. Solid-State Circuits*, vol 37, no. 12, pp. 1618-1627, Dec. 2002.

[2] K. Dyer et al., "An Analog Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1904-1911, Dec., 1998.

[3] K. Poulton et al., "A 20GS/s 8b ADC with a 1MB Memory in 0.18μm CMOS", *ISSCC Dig. Tech. Papers*, pp. 318-319, Feb., 2003

[4] S. Gupta and O. Zabroda, "High Speed Sampling Architectures", Teranetics Approved Patent Application, Filed at USPTO, Jan 12th 2005.

[5] W. Yang et al., "A 3-V 340mW 14-b 75-MSample/s CMOS ADC with 85-dB SFDR at Nyquist Input", *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1931-1936, Dec. 2001.

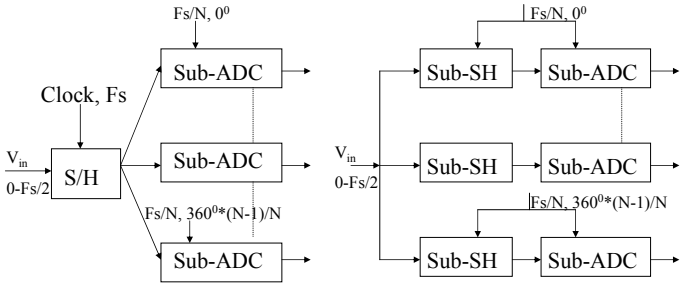

Figure 31.6.1: Two conventional architectures for time-interleaved converters.

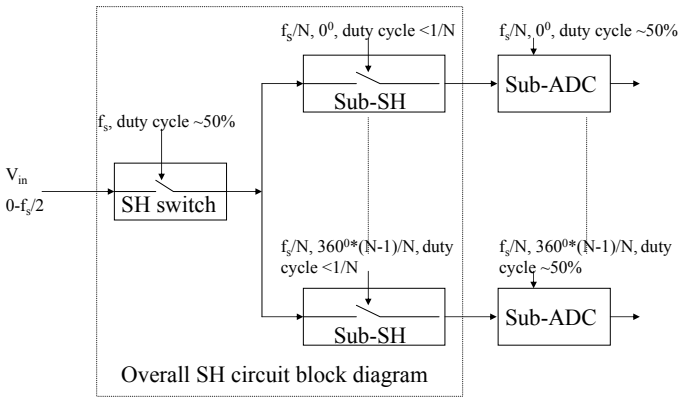

Figure 31.6.2: The proposed time-interleaved ADC architecture block diagram.

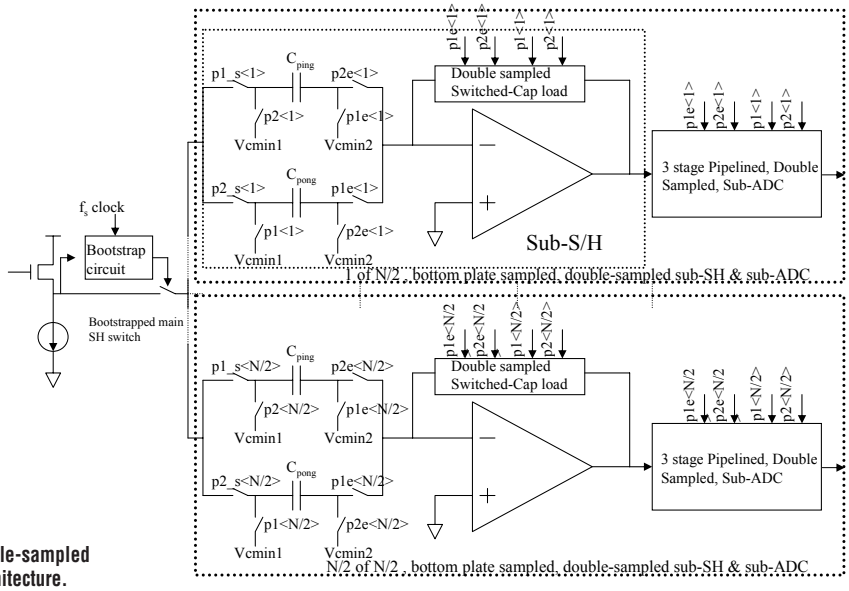

Figure 31.6.3: Proposed double-sampled time-interleaved ADC circuit architecture.

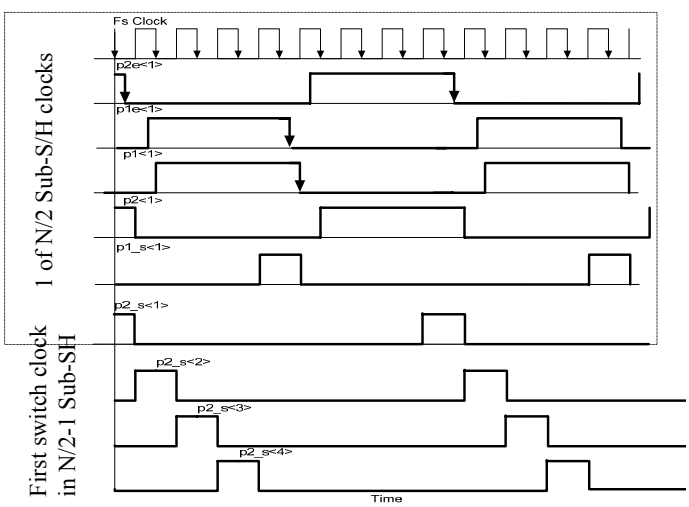

Figure 31.6.4: Clocks showing Sub-S/H clocks and 1GS/s f_s clock.

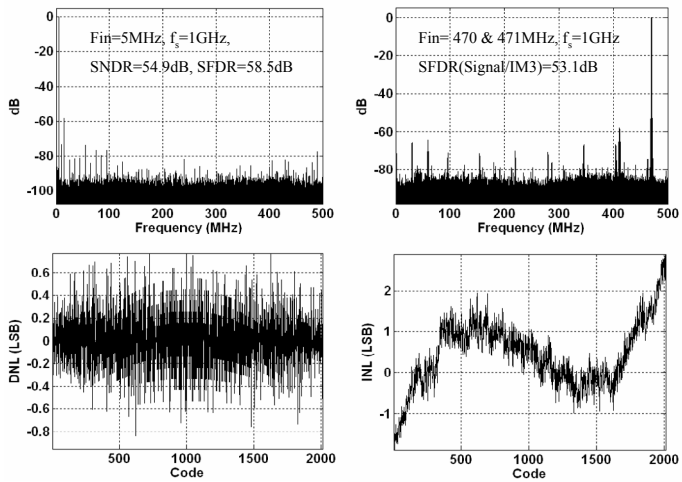

Figure 31.6.5: Measured FFTs at 5MHz and at 470 and 471MHz (dual tone) inputs, and DNL, and INL.

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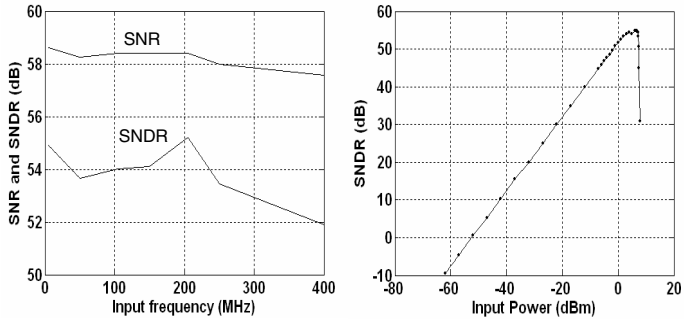

Figure 31.6.6: Measured SNDR versus input amplitude and frequency.

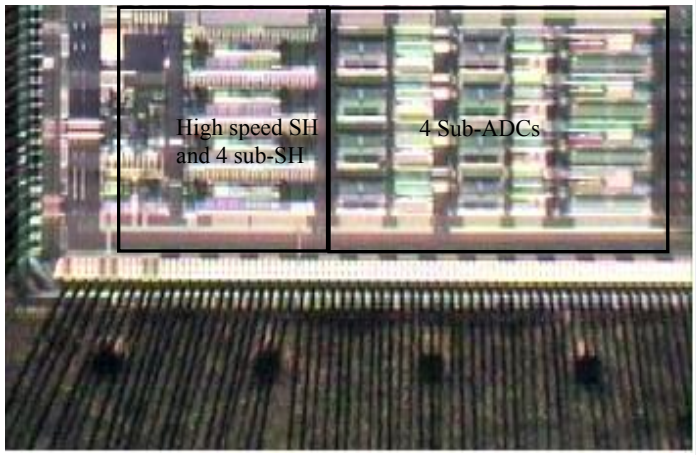

Figure 31.6.7: Zoomed in micrograph of the chip showing 1GS/s ADC.

